REFERENCE MANUAL

Model 2108

TX04/RX04
Interconnect Modules

Revision Date: 8/24/07
Manual Part Number: 2108RM006
Instrument Part Number:
405307-002/405306-002

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- Don't repair the instrument unless you are a qualified electronics technician and have instructions from Talon Instruments.
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- Pay attention to the **CAUTION** statements. They point out situations that can cause equipment damage.
- Use ESD static control procedures when handling the 2108 or any of its modules.

Table of Contents

1 TX04/RX04 Interconnect Modules 1
1.1 2108 TX04 Module 1-1
1.2 2108 RX04 Module 1-1
2 Specifications 2
2.1 General 2-1
2.2 Environmental 2-2
2.3 Power Requirements 2-2
2.3.1 VXI Power Requirements 2-2
3 Jumpers/Testpoints 3
3.1 TX04 Jumpers/Testpoints 3-1
3.1.1 2108 TX04 Test Point Description 3-1
3.1.2 2108 TX04 Jumper Description 3-1
3.1.2.1 Channel Voltage Daisy Chain (J3, J4) 3-1
3.2 RX04 Jumpers/Testpoints 3-2
3.2.1 2108 RX04 Test Point Description 3-2
3.2.2 2108 RX04 Jumper Description 3-2
3.2.2.1 Channel Voltage Daisy Chain (J3, J4) 3-2
4 Front Panel 4
4.1 TX04 Front Panel 4-1
4.1.1 TX04 Front Panel LED 4-1
4.1.2 TX04 Front Panel SMA 4-1
4.1.3 TX04 Front Panel I/O 4-1
4.2 RX04 Front Panel 4-2
4.2.1 RX04 Front Panel LED 4-2
4.2.2 RX04 Front Panel SMA 4-3
4.2.3 RX04 Front Panel I/O 4-3
5 Functional Description 5
5.1 TX04 5-1
5.1.1 TX04 Output Signals 5-1
5.1.1.1 TTL Outputs 5-1
5.1.1.2 Bi-Directional Capabilities 5-1
5.1.2 2108TX04 Inputs 5-1
5.1.2.1 Clock Inputs 5-1
5.1.2.2 TTL Inputs 5-1
5.2 RX04 5-2
5.2.1 RX04 Input Signals 5-2
5.2.1.1 Clock Inputs 5-2
5.2.1.2 Bi-directional Capabilities 5-2
5.2.2 TTL Outputs 5-2
5.2.3 LED Indicator 5-3
5.2.4 Self-Clocking Data 5-3
Appendix A Glossary . . . . . A

Appendix B Register Description . . . . . B
1 TX04 Register Map B-1
1.1 Control/Status Register (CSREG, RW:108000_h) B-1
1.2 Test/LED Register (TEST, R/W:170008_h) B-2
1.3 Module Identification (MID, R:178000_h). B-2
2 RX04 Register Map B-2
2.1 Control Register (CSREG, RW:108000_h) B-2
2.2 Test/LED Register (TEST, R/W:170008_h) B-3
2.3 Module ID (MID, R:178000_h) B-3

List of Figures

Figure 1-1 2108 TX04 Front View 1-1
Figure 1-2 TX04 Bottom View 1-1
Figure 1-3 RX04 Bottom View 1-1
Figure 1-4 RX04 Front View 1-1
Figure 3-1 2108 TX04 Jumper/Testpoint Location 3-1
Figure 3-2 2108 RX04 Jumper/Testpoint Location 3-2
Figure 4-1 TX04 Front Panel 4-1
Figure 4-2 RX04 Front Panel 4-2

List of Tables

Table 2-1 VXI Backplane Power Requirements 2-2
Table 3-1 2108 TX04 Test Point Description 3-1
Table 3-2 2108 RX04 Test Point Description 3-2
Table 4-1 TX04 I/O Connector Pinout. 4-2
Table 4-2 RX04 I/O Connector Pinout 4-3
Table 5-1 TX04 Clock Input Description 5-1
Table 5-2 RX04 Clock Input Description. 5-2
Table B-1 TX04 Register Segment List B-1
Table B-2 TX04 Control/Status Bit Description. B-1
Table B-3 TX04 Module Identification Bit Description. B-2
Table B-4 RX04 Control Register Bit Description B-2
Table B-5 Test/LED Bit Definitions B-2
Table B-6 Test/LED Bit Definitions B-3
Table B-7 Module Identification Register Bit Description B-3

1 TX04/RX04 Interconnect Modules

Just as each serial interface has unique data format and bit format characteristics, each interface also has unique electrical line driver/receiver characteristics. These characteristics vary from output voltage levels, output slew rates, bipolar or trinary signals, differential output signals and more. The TX04 and RX04 were developed to address LVDS differential signaling.

1.1 2108 TX04 Module

The TX04 shown below provides 8 LVDS outputs. The Transmitter Interconnect Modules provide the user with drivers to meet the electrical requirements of the UUT. Custom modules can be easily deleloped if off-the-shelf modules do not meet the user's requirements.

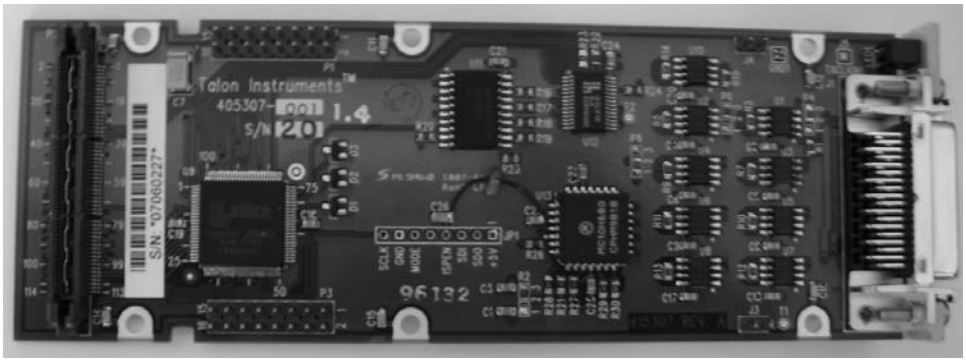

Figure 1-2 TX04 Bottom View

Figure 1-1 2108 TX04 Front View

1.2 2108 RX04 Module

The RX04 supports LVDS differential. The Receiver Interconnect Modules provide for the physical connection to the UUT. The RX04 shown below provides a single channel for recording serial data. Alternately, the physical interconnect can be supplied from the TX04 in the bi-directional mode.

Figure 1-3 RX04 Bottom View

Figure 1-4 RX04 Front View

2 Specifications

The following sections list the specifications of the 2108 TX04/RX04 modules.

2.1 General

TX04

- TxSig Outputs
  - Configuration TxSig1-TxSig8 ..... LVDS - SN65LVDM176D
  - Differential driver output Voltage (with 100ΩTermination) 650mV
  - Differential driver output Voltage (50 Ω load total) 350mV
  - Differential receiver threshold ..... -50mV min, +50mV max
  - Differential receiver common mode range ..... 50mV to +2.5V
  - Output Impedance 100Ω
  - Max Bit Rate 200Mbps
- TxClkIn1
  - Configuration ..... Single Ended ECL - MC10H680
  - Input Impedance ..... 51Ω to -2V
  - Frequency max. 175MHz
- TxClkIn2
  - Configuration ..... LVDS - SN65LVDM176D
  - Differential data rate ..... 200 Mb/s
  - Differential receiver threshold ..... -50mV min, +50mV max
  - Differential receiver common mode range ..... 50mV to +2.5V
  - Input Impedance 100Ω
- TxClkIn3
  - Configuration ..... Differential ECL - MC10H680
  - Input Impedance ..... 51Ω to -2V
  - Frequency max. 200MHz
- TxClkIn4
  - Configuration ..... Single Ended TTL - SN74AS244
  - Input Impedance ..... 82Ω to Gnd
  - Frequency max. 50MHz
- TxBusy
- TxSyncPulse
  - Configuration ..... Single Ended TTL - SN74AS244
  - Output Impedance ..... 47Ω Series
- TxFlagIn1
- TxFlagIn2
  - Configuration ..... Single Ended TTL - SN74AS244
  - Input Termination ..... None

RX04

- RxData Inputs
  - Configuration ..... LVDS - SN65LVDM176D
  - Differential data rate ..... 200 Mb/s
  - Differential receiver threshold ..... -50mV min, +50mV max
  - Differential receiver common mode range ..... 50mV to +2.5V
  - Input Impedance 100Ω
- RxClkIn1
  - Configuration ..... Single Ended ECL - MC10H680
  - Input Impedance ..... 51Ω to -2V
  - Frequency max. 175MHz
- RxClkIn2
  - Configuration ..... LVDS - SN65LVDM176D
  - Differential data rate ..... 200 Mb/s
  - Differential receiver threshold ..... -50mV min, +50mV max
  - Differential receiver common mode range ..... 50mV to +2.5V
  - Input Impedance 100Ω
- RxClkIn3
  - Configuration ..... Differential ECL - MC10H680
  - Input Impedance ..... 51Ω to -2V
  - Frequency max. 200MHz
- RxClkIn4
  - Configuration ..... Single Ended LV TTL - 22LV10
  - Input Impedance ..... 82Ω to Gnd
  - Frequency max. 50MHz
- RxSig1
- RxSig2
- RxTrigNum0
- RxTrigNum1
- RxTrigNum2
- RxTrigNum3
- RxTrigValid

Configuration .....Single Ended TTL - SN74AS244
Output Impedance .....47Ω Series

RxG1Val
RxG0Val
RxClkOut

Configuration .....Single Ended LVTTL - 22LV10
Output Impedance .....47Ω Series

2.2 Environmental

Temperature Range

Operating	0° C to +50° C
Storage	-40° C to +70° C (RH not controlled)

Altitude

Operating	Sea level to 10,000 ft.
Storage	Sea level to 40,000 ft.

Relative Humidity (non condensing)

0°C to +10°C	not controlled
+11°C to +30°C	95+/-5%RH
+31°C to +40°C	75+/-5%RH
+41°C to +50°C	45+/-5%RH

2.3 Power Requirements

The following sections describe the VXI and front panel power requirements of the 2108 TX04 and RX04 interconnect modules.

2.3.1 VXI Power Requirements

The VXI backplane power requirements are listed in table 2-1 below.

Voltage	TX04	RX04
	Peak (Amps)	Peak (Amps)
+5V	TBD	TBD
-5.2V	TBD	TBD
-2V	TBD	TBD
+12V	0	0
-12V	0	0
+24V	0	0
-24V	0	0

Table 2-1 VXI Backplane Power Requirements

3 Jumpers/Testpoints

The following sections describe the jumpers for the 2108 TX04 and RX04 modules.

3.1 TX04 Jumpers/Testpoints

Figure 3-1 below shows the location of the jumpers and test points on the 2108 TX04 UUT interconnect module PCB, part number 30121 revision 'A'.

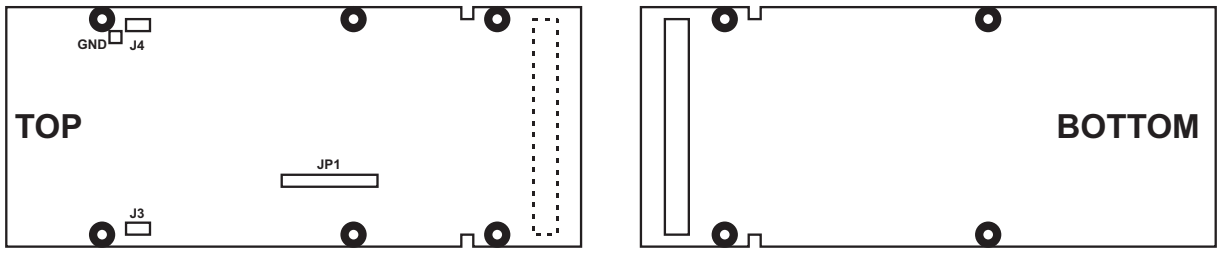

Figure 3-1 2108 TX04 Jumper/Testpoint Location

3.1.1 2108 TX04 Test Point Description

Table 3-1 describes the test points on the 2108 TX04.

Mnemonic	Description
GND	Probe Signal Ground.
JP1	In-circuit Program Port for U6.

Table 3-1 2108 TX04 Test Point Description

3.1.2 2108 TX04 Jumper Description

The following sections describe the 2108 TX04 jumpers.

3.1.2.1 Channel Voltage Daisy Chain (J3, J4)

These jumpers allow the voltage buses (V+ and V-) to be chained between adjacent modules. The TX04 does not use these voltages so this bus is included for compatibility with programmable modules.

Factory default: Daisy chain not connected.

To connect the front panel power bus to adjacent transmitter channels install shunts between pin 1 and 2 to pin 1 and 2 of the adjacent transmitter interface module daisy chain jumper.

3.2 RX04 Jumpers/Testpoints

Figure 3-2 below shows the location of the jumpers and test points on the 2108 RX04 UUT interface module PCB, part number 30221 revision 'NC'.

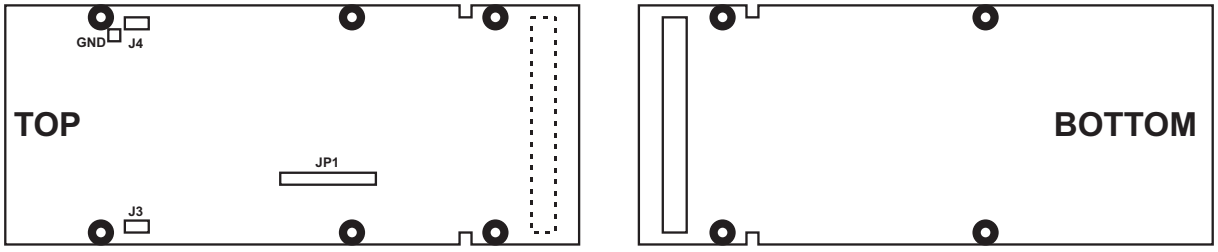

Figure 3-2 2108 RX04 Jumper/Testpoint Location

3.2.1 2108 RX04 Test Point Description

Table 3-2 describes the test points on the 2108 RX04.

Mnemonic	Description
GND	Probe Signal Ground.
JP1	In-circuit Program Port for U6.

Table 3-2 2108 RX04 Test Point Description

3.2.2 2108 RX04 Jumper Description

The following sections describe the 2108 RX04 jumpers.

3.2.2.1 Channel Voltage Daisy Chain (J3, J4)

These jumpers allow the voltage buses (V+ and V-) to be chained between adjacent modules. The TX04 does not use these voltages so this bus is included for compatibility with programmable modules.

Factory default: Daisy chain not connected.

To connect the front panel power bus to adjacent transmitter channels install shunts between pin 1 and 2 to pin 1 and 2 of the adjacent transmitter interface module daisy chain jumper.

4 Front Panel

The following describes the pinout and signal description of the Model 2108 TX04/RX04 UUT interconnect modules.

4.1 TX04 Front Panel

Figure 4-1 below illustrates the TX04 front panel.

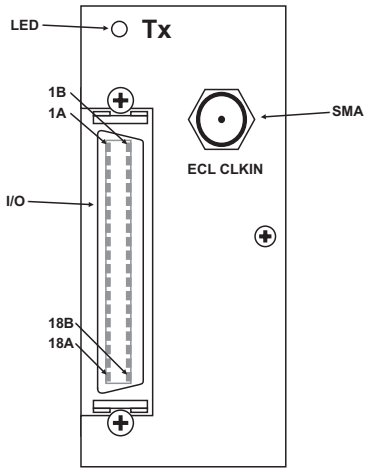

Figure 4-1 TX04 Front Panel

The TX04 front panel is comprised of three elements, LED, SMA, I/O.

The following sections describes each of these elements.

4.1.1 TX04 Front Panel LED

The front panel LED indicator displays the following condition:

GREEN The 2108TX is currently transmitting a CMT in the RUN state.

4.1.2 TX04 Front Panel SMA

The front panel SMA is used to input the single ended ECL clock input signal (TxClkIn1).

4.1.3 TX04 Front Panel I/O

The front panel I/O connector (AMP P/N “2-178238-5”) is used to connect the 2108 to the UUT/ITA fixture.

Talon sells a shielded twisted pair three foot cable assembly P/N “2108/300” that has a mating connector on one side and open ended on the other.

Table 4-1 below list the pinout of the TX04 I/O connector.

Pin Number	Signal	Default Source	Description
2A	TxSig1+	TxData+	Positive Transmitter Data
3A	TxSig1-	TxData-	Negative Transmitter Data
4A	TxSig2+	TxClkOut+	Positive Transmitter Clock
5A	TxSig2-	TxClkOut-	Negative Transmitter Clock
6A	TxSig3+	TxMarker1+	Static enable programmable output.
7A	TxSig3-	TxMarker1-	Static enable programmable output.
8A	TxSig4+	TxMarker2+	Static enable programmable output.
9A	TxSig4-	TxMarker2-	Static enable programmable output.
10A	TxSig5+	TxFlagOut1+	Static enable programmable output.
11A	TxSig5-	TxFlagOut1-	Static enable programmable output.
12A	TxSig6+	TxFlagOut2+	Static enable programmable output.
13A	TxSig6-	TxFlagOut2-	Static enable programmable output.
14A	TxSig7+	TxSyncPulse+	Static enable programmable output.
15A	TxSig7-	TxSyncPulse-	Static enable programmable output.
16A	TxSig8+	TxBusy+	Static enable programmable output.
17A	TxSig8-	TxBusy-	Static enable programmable output.
18A	TxClkIn3+		Differential ECL clock input positive input.
2B	TxFlagIn1		TTL Input flag one.
4B	TxFlagIn2		TTL Input flag two.
6B	TxClkIn2+		LVDS clock positive input.
8B	TxClkIn2-		LVDS clock negative input.
10B	TxBusy		TTL transmitter busy flag.
12B	TxSyncPulse		TTL Transmitter sync pulse flag.
14B	TxClkIn4		Single ended TTL clock input
18B	TxClkIn3-		Differential ECL clock input negative input.
All other pins signal ground.			

Table 4-1 TX04 I/O Connector Pinout

4.2 RX04 Front Panel

Figure 4-2 below illustrates the RX04 front panel.

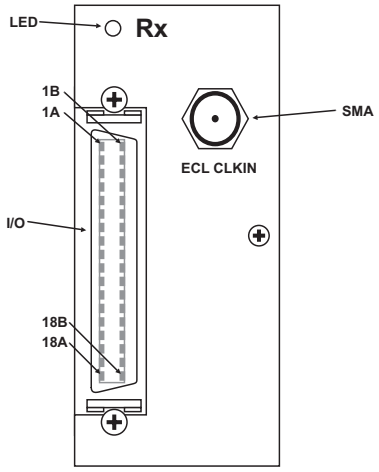

Figure 4-2 RX04 Front Panel

The RX04 front panel is comprised of three elements, LED, SMA, I/O.
The following sections describes each of these elements.

4.2.1 RX04 Front Panel LED

The front panel LED is a bi-colored indicator of the following conditions:

AMBER The 2108RX is currently waiting for a trigger (armed).

GREEN The 2108RX has detected a valid trigger and recording post trigger data.

The front panel LED will only be active if RxBusy is selected as RxSig2 and RxArm as RxSig1.

4.2.2 RX04 Front Panel SMA

The front panel SMA is used to input the single ended ECL clock input signal (RxClkIn1).

4.2.3 RX04 Front Panel I/O

The front panel I/O connector (AMP P/N “2-178238-5”) is used to connect the 2108 to the UUT/ITA fixture.

Talon sells a shielded twisted pair three foot cable assembly P/N “2108/300” that has a mating connector on one side and open ended on the other.

Table 4-2 below list the pinout of the RX04 I/O connector.

Pin Number	Signal	Default Source	Description
2A	RxData+		Positive data input.
4A	RxData-		Negative data input.
6A	RxClkIn2+		Positive clock input
8A	RxClkIn2-		Negative clock input
10A	RxQual1+		Positive qualifier one.
12A	RxQual1-		Negative qualifier one.
14A	RxQual2+		Positive qualifier two.
16A	RxQual2-		Negative qualifier two.
17A	RxClkIn3+		Differential ECL clock input positive input.
18A	RxSig1	RxArm	TTL receiver signal 1.
2B	RxTrigValid		TTL trigger valid flag.
4B	RxTrigNum0		TTL trigger number zero.
6B	RxTrigNum1		TTL trigger number two.
8B	RxTrigNum2		TTL trigger number three.
10B	RxTrigNum3		TTL trigger number four.
12B	RxG0Val		LVTTL receiver good zero data.
14B	RxG1Val		LVTTL receiver good one data.
15B	RxClkIn4		Single ended LVTTL clock input
16B	RxClkOut		LVTTL receiver clock.
17B	RxClkIn3-		Differential ECL clock input negative input.
18B	RxSig2	RxBusy	TTL receiver signal 2.

Table 4-2 RX04 I/O Connector Pinout

5 Functional Description

The following sections describe the TX04/RX04 functionality.

5.1 TX04

The TX04 is a UUT interconnect module for the 2108TX transmitter module. It mounts on the 2108 Baseboard and provides the I/O translation between the UUT and the 2108TX module.

The TX04 provides LVDS differential I/O.at up to 50 Mb/s

5.1.1 TX04 Output Signals

There are eight LVDS differential outputs (TxSig1 through TxSig8) for the 2108TX04 and two TTL outputs (TxBusy and TxSyncPulse). TxSig1 and TxSig2 have dynamic enables while TxSig3 through TxSig8 have static enables.

The choices for each signal are the true or complemented state of the following:

- TxData
- TxMarker1
- TxMarker2
- TxFlagOut1
- TxFlagOut2
- TxClkOut
- TxStrobe
- TxBusy
- TxSyncPulse

5.1.1.1 TTL Outputs

There are two TTL driven outputs, TxBusy and TxSyncPulse driven by a 74AS244.

5.1.1.2 Bi-Directional Capabilities

The TxSig1 Output can be programmatically routed over to the adjacent 2108RX04 Data Input. This permits bi-directional communication with the users UUT over one data line. The selected clock input can also be programmatically routed over to the adjacent 2108RX04.

5.1.2 2108TX04 Inputs

There are four clock inputs (TxClkIn1 - TxClkIn4) and two TTL Flag Inputs (TxFlagIn1 and TxFlagIn2).

5.1.2.1 Clock Inputs

The following table lists the clock inputs and logic/termination descriptions.

TX04 Clock Inputs	Descriptions	Impedance
TxClkIn1	ECL Single Ended	51Ω to -2V
TxClkIn2	LVDS differential	100Ω parallel
TxClkIn3	ECL Differential	51Ω to -2V
TxClkIn4	TTL Single Ended	100Ω to GND

Table 5-1 TX04 Clock Input Description

5.1.2.2 TTL Inputs

The Flag Inputs are standard TTL compatible inputs.

5.2 RX04

The RX04 is a UUT interconnect module for the 2108RX receiver module. It mounts on the 2108 Baseboard and provides the I/O translation between the UUT and the 2108RX.

5.2.1 RX04 Input Signals

There are five differential inputs on the 2108RX04: RxData, RxClkIn2, RxQual1, RxQual2 and RxClkin2. Additionally, there are three other clock input selections; a single ended ECL, a differential ECL, and a single ended TTL.

5.2.1.1 Clock Inputs

The following table lists the clock inputs and logic/termination descriptions.

RX04 Clock Inputs	Description	Impedance
RxClkin1	ECL Single Ended	51Ω to -2V
RxClkin2	LVDS differential	100Ω parallel
RxClkin3	ECL Differential	51Ω to -2V
RxClkin4	TTL Single Ended	100Ω to GND
TxClkIn	Selected TxClkIn<n> Clock	From adjacent TX04
TxClkOut	Selected Transmitter Clock	From adjacent TX04

Table 5-2 RX04 Clock Input Description

5.2.1.2 Bi-directional Capabilities

A bi-directional mode of operation can be configured with the adjacent 2108TX04. When the 2108TX04 is in bi-directional mode, i.e. it has been programmed to enable the intermodule data and clock, the 2108RX04 can be programmed to select these inputs instead of its own front panel data and clock signals.

5.2.2 TTL Outputs

There are ten TTL outputs from the 2108RX04:

RxClkOut	RxTrigValid
RxG1Val	RxTrigNum0
RxG0Val	RxTrigNum1
RxSig1	RxTrigNum2
RxSig2	RxTrigNum3

The first three are driven by very fast, low skew, LVTTL drivers. The others are driven by a 74AS244. There's a programmable enable for these two groups of outputs so they may be turned off if not in use. The RxClkOut, RxG1Val and RxG0Val are especially useful, in that they are outputs from the 2108RX showing the digital signals which were derived from the input RxData and RxClkIn (via the amplifiers and comparators). Adjustable delay elements in the 2108Rx allow RxData and RxClkIn to be precisely aligned.

The trigger outputs (RxTrigValid, RxTrigNnum0, RxTrigNum1, RxTrigNum2, RxTrigNum3) indicate when a trigger occurs and the trigger number. RxSig1 and RxSig2 outputs are user selectable in the 2108Rx and described below:

RxSig1:

RxArm (default)	Record sequence running and waiting for trigger.
RxBusy	Record sequence running.
RxWait	Waiting for TxACK from transmitter.
TxAck	Acknowledge signal from transmitter.
LostClk	Clocks error signal.
HFCR-ERR	High frequency clock recovery error.
MemABsy	Record memory bank A busy.
LFCR-DEV	Low frequency clock recovery deviation (too slow or fast).

RxSig2:

RxArm	Record sequence running and waiting for trigger
RxBusy (default)	Record sequence running.
TrigDis	Trigger disabled (post trigger or waiting for TxACK).
TxAck	Acknowledge signal from transmitter.
LostClk	Clocks error signal.
HFCR-ND	High frequency clock recovery error. Not enough data.
MemBBsy	Record memory bank B busy.
LFCR-ERR	Low frequency clock recovery deviation error.

5.2.3 LED Indicator

When RxSig1 is chosen to be “RxArm” and the RxSig2 is chosen to be “RxBusy”, the LED will be Green when “BUSY” and Amber if “ARMED” and “BUSY”.

5.2.4 Self-Clocking Data

The 2108RX has built in capabilities to recover a clock from the input DATA. Consult the 2108RX description for further details.

Appendix A Glossary

Bipolar	One signal represents a state.
Comparator	Compares an input signal with a reference level.
Differential	A pair of signals represent a state. Also, when one is at a high level the other is at a low level and vice-versa.
ECL	Emitter Coupled Logic.
FlagIn	An input signal which the transmitter can query.
FlagOut	An output signal (level or pulse) which the transmitter can generate.
Good “0”	A signal generated when an input signal is a valid low.
Good “1”	A signal generated when an input signal is a valid high.
HRCR	High Frequency Clock Recovery.
LED	Light Emitting Diode.
LFCR	Low Frequency Clock Recovery.
Marker	An output signal used to mark one or more portions of the output data stream.
Reference	A programmable DC voltage.
RX04	Type 4 Receiver Interconnect Module.
RxArm	Record sequence “ARMed” and waiting for a trigger.
RxBusy	Record sequence running.
RxCLKOUT	An output signal derived from “Clock In” (used to align data wrt clock).
RxG0Val	An output signal derived from “Good-0” (used to align data wrt clock).
RxG1Val	An output signal derived from “Good-1” (used to align data wrt clock).
RxTrigNumber	The particular trigger number which occurred for a particular trigger event.
RxTrigValid	Trigger valid signal generated by the receiver when a trigger has occurred.
RxWait	Receiver is waiting for an acknowledge of a Trig Valid.
SMA	A small screw-on RF connector.
SyncPulse	An output pulse which can be positioned in relation to the output data stream (typically used to synchronize another instrument).
TrigDis	Trigger disabled in the receiver (in post trigger or waiting for a TxAck).
Tri-state	From the drivers view this is a passive-non driven state that is high impedance. From the receivers view this is a state between VIL and VIH.
TX04	Type 4 Transmitter Interconnect Module.
TxAck	A signal from the transmitter sent to the receiver acknowledging that a trigger has been captured.
TxBusy	Transmitter running.
TxCLKOUT	Selected clock being output by the transmitter (can be inverted and delayed).
UUT	Unit Under Test.

Appendix B Register Description

The following sections describes the register maps of the TX04 and RX04 interface modules.
Both the TX04 and the RX04 register segments are located in the “IFCREG” major segment, 100000h.

1 TX04 Register Map

The TX04 register segments are described below:

Register Segment Code (RSC)				Register Segment Name	Base Address IFCREG + RSC	Description
A18	A17	A16	A15			
0	0	0	1	CSREG	108000h	Control/Status Register
1	1	1	0	TEST	170008h	Test/LED Registers
1	1	1	1	MID	178000h	Module ID

Table B-1 TX04 Register Segment List

1.1 Control/Status Register (CSREG, RW:108000_h)

Table B-2 lists the bit description of the Control/Status register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU														S1B	NU			LED	NU	IMCE	CS2	CS1	CS0	S8EN	S7EN	S6EN	S5EN	S4EN	S3EN	S2EN	S1EN

Table B-2 TX04 Control/Status Bit Description

Field Bit Definition:

S1EN-S8EN Driver enable (1 = enabled, 0 = disabled).
CS0-CS2 Clock Select Code

Bit 10	Bit 9	Bit 8	Clock
0	0	0	Disabled
0	0	1	TxClkIn1 (ECL Single Ended)
0	1	0	TxClkIn2 (Differential LVDS)
0	1	1	TxClkIn3 (ECL Differential)
1	0	0	TxClkIn4 (TTL Single Ended)
1	1	1	Test Clock (16MHz), see note 1

IMCE Inter module clock enable. (1 = enabled, 0 = disabled).
S1B Signal One Bidirectional enable (1 = enabled, 0 = disabled).
LED LED Enable (1 = drives the front panel LED), see note 1.

Notes:

1. Bit 0 of the TEST register must be set high.

1.2 Test/LED Register (TEST, R/W:170008_h)

Table B-5 lists the bit description of the test/led register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU												TEST4	TEST2	TEST2	TEST1

Table B-5 Test/LED Bit Definitions

Field/Bit Definition:

TEST1	1 = LED test and TSTCLKEN, 0 = Normal Operation, see note 1.
TEST2	1 = IRQ test, 0 = Normal Operation.
TEST3	1 = TRIGB test, 0 = Normal Operation.
TEST4	Read TRIGA level.

Notes:

None

1.3 Module Identification (MID, R:178000_h)

The revision register contains the transmitter front end revision/status code.

Table B-3 lists the bit description of the module identification register:

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								T/R	T/P	ID					

Table B-3 TX04 Module Identification Bit Description

Field Bit Definition:

ID	Identification Code
T/P	Test/Production flag (1 = Test, 0 = Production).
T/R	Transmit/Receive (1 = Receiver, 0 = Transmitter).

Notes:

1. A read of the MID register for the TX04 will return a ‘5’.

2 RX04 Register Map

The RX04 register segments are described below:

2.1 Control Register (CSREG, RW:108000_h)

Table B-4 lists the bit description of the control register.

Bit #																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU											LED	NU		OE1	OE0	CS2	CS1	CS0	NU			IMEN	NU							

Table B-4 RX04 Control Register Bit Description

Field Bit Definition:

IMEN	Data Enable (0 = Data source is front panel, 1 = Data source is Tx IM)
CS0-CS2	Clock select:

Bit 10	Bit 9	Bit 8	Clock
0	0	0	Disabled
0	0	1	RxClkIn1 (ECL Single Ended)
0	1	0	RxClkIn2 (Differential LVDS)
0	1	1	RxClkIn3 (ECL Differential)
1	0	0	RxClkIn4 (TTL Single Ended)
1	0	1	Inter Module Clock
1	1	0	Transmitter Clock

OE0 Output Enable (RxSIG1, RxSIG2, RxTRIGVALID, RxTRIGNUM (1 = enabled, 0 = disabled).
OE1 Output Enable 1 (RxCLKOUT, RxG1VAL, RxG0VAL (1 = enabled, 0 = disabled).
LED Front panel led enable (1 = enabled, 0 = disabled).

Notes:

1. LED should only be enabled if RxSig1 = RxArm and RxSig2 = RxBusy.

2.2 Test/LED Register (TEST, R/W:170008_h)

Table B-5 lists the bit description of the test/led register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU												TEST4	TEST2	TEST2	TEST1

Table B-6 Test/LED Bit Definitions

Field/Bit Definition:

TEST1 1 = LED test and TSTCLKEN, 0 = Normal Operation, see note 1.
TEST2 1 = IRQ test, 0 = Normal Operation.
TEST3 1 = TRIGB test, 0 = Normal Operation.
TEST4 Read TRIGA level.

Notes:

1. Bit 13 of CSREG will toggle the front panel LED.

2.3 Module ID (MID, R:178000_h)

Table B-7 lists the bit description of the ID register.

Bit #															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU								T/R	T/P	ID					

Table B-7 Module Identification Register Bit Description

Field Bit Definition:

ID Identification code.
T/P Test/Production flag (1 = Test, 0 = Production).
T/R Transmit/Receive (1 = Receiver, 0 = Transmitter).

Notes:

1. A read of the MID register for the RX04 will return a '133', 85_h.